top surface of the semiconductor substrate **100**. The conductive layer **134** in the contact hole **125** may have a fifth thickness T**5**, when measured in the first direction D**1** or the second direction **1**)**2**. Since the conductive layer **134** is formed by a deposition method with a poor step coverage property (e.g., PVD process), the second thickness T**2** may be greater than the fifth thickness T**5**.

[0116] In some example embodiments, the barrier layer **132** may be formed of or include at least one of Ti or TiN. The conductive layer **134** may be formed of or include a metallic material (e.g., containing aluminum (Al)).

[0117] Referring to FIGS. **2** and **10**, a second photoresist pattern PR may be formed on the conductive layer **134**. In some example embodiments, a plurality of second photoresist patterns PR may be formed to define positions and shapes of the redistribution layers **130** described with reference to FIGS. **2** and **3**.

[0118] The conductive layer **134** and the barrier layer **132** may be etched, for example sequentially etched using the second photoresist pattern PR as an etch mask to form the redistribution layer **130**. The etching process of the conductive layer **134** and the barrier layer **132** may be performed using a dry etching process. As an example, an etching gas containing BCl_3 and/or SF_6 may be used for the dry etching process, but the inventive concepts may not be limited thereto. The redistribution layer **130** may include a barrier pattern **133** and a conductive pattern **135** on the barrier pattern **133**. The conductive pattern **135** may include a contact portion **135***a*, a conductive line portion **135***b*, and a bonding pad portion **135***c*.

[0119] In the case where the second photoresist pattern PR is used as a common mask for forming the conductive pattern **135** and the barrier pattern **133**, the conductive pattern **135** and the barrier pattern **133** may overlap each other, when viewed in a plan view. Accordingly, the conductive pattern **135** and the barrier pattern **133** may be formed to have sidewalls aligned with each other in plan view.

[0120] An upper portion of the lower insulating structure **120** may be etched during the process of etching the conductive layer **134** and the barrier layer **132**. For example, during the etching process, the conductive layer **134** and the barrier layer **132** exposed by the second photoresist pattern PR. may be removed, and then, a portion of the third lower insulating layer **120***c* thereunder may be at least partially etched. As a result, during the process of etching the redistribution layer **130**, a recess region RC may be formed in the third lower insulating layer **120***c*. Here, the recess region RC may be formed to have a bottom surface that is lower than the top surface of the third lower insulating layer **120***c* provided under the redistribution layer **130**.

[0121] Referring to FIGS. **2** and **11**, a remaining portion of the second photoresist pattern PR may be selectively removed, Thereafter, an upper insulating structure **140** may be formed on the redistribution layer **130** and the lower insulating structure **120**.

[0122] For example, the formation of the upper insulating structure **140** may include forming, for example sequentially forming an upper insulating layer **140***a* and a polymer layer **140***b* on the semiconductor substrate **100**. The upper insulating layer **140***a* may be formed via, for example, an atomic layer deposition (ALD) process or a chemical vapor deposition (CVD) process. The polymer layer **140***b* may be formed by coating a polymer material (e.g., at least one of polyimide, fluoro carbon, resin, or synthetic rubber) or a precursor thereof on the upper insulating layer **140***a*. The upper insulating layer **140***a* may be formed to have a third thickness **13**, and the polymer layer **140***b* may be formed to have a fourth thickness T**4**. Here, the fourth thickness T**4** may be greater than the third thickness T**3**.

[0123] Referring to FIGS. **2** and **3**, the upper insulating structure **140** may be patterned to form a first opening **145** exposing the bonding pad portion **135***c*. The patterning of the upper insulating structure **140** may include forming a third photoresist pattern (not shown) and etching the upper insulating structure **140** using the third photoresist pattern as an etch mask, where the third photoresist pattern is formed to define an opening overlapped with the bonding pad portion **135***c*. The first opening **145** may be formed to have a third width W**3**. For example, the third width W**3** may range from about 100 μm to about 300 μm. In a subsequent package process, a wire bonding process may be performed on the bonding pad portion **135***c* exposed by the first opening **145**.

[0124] According to some example embodiments of the inventive concepts, the redistribution layer **130** may be formed of or include a less expensive metal (e.g., aluminum) than gold or copper, and thus, it is possible to reduce production cost in a process of fabricating a semiconductor chip. In addition, the redistribution layer **130** may be formed by a deposition and a patterning process instead of by a plating process, and thus, this may make it possible to use the existing metal patterning system for the process of forming the redistribution layer **130**. Accordingly, it is possible to improve process efficiency in the fabrication process.

[0125] Furthermore, in a fabrication method according to some example embodiments of the inventive concepts, a plurality of air gaps AG may be formed in the lower insulating structure. The presence of the air gaps AG may reduce an effective dielectric constant of the lower insulating structure **120**.

[0126] FIG. **12** is a sectional view of sections, which are respectively taken along lines I-I' and II-II' of FIG. **2**, and illustrates a first semiconductor chip according to some example embodiments of the inventive concepts. In the following description, an element of the first semiconductor chip previously described with reference to FIGS. **2** to **4**B may be identified by a similar or identical reference number without repeating an overlapping description thereof, for the sake of brevity.

[0127] Referring to FIGS. **2** and **12**, a second opening **146** may be provided to penetrate the upper insulating structure **140** and expose the contact portion **135***a*. The second opening **146** may have a fifth width W**5**. In some example embodiments, the fifth width W**5** may range from about 10 μm to about 100 μm.

[0128] Although not shown, an additional outer terminal may be coupled to the contact portion **135***a* through the second opening **146**. Accordingly, this structure of the contact portion **135***a*, in conjunction with the bonding pad portion **135***c* exposed by the first opening **145**, may make it possible to increase a degree of freedom in establishing a routing path with an external controller (not shown).

[0129] FIG. **13** is a sectional view of sections, which are respectively taken along lines **14'** and of FIG. **2**, and illustrates a first semiconductor chip according to some example embodiments of the inventive concepts. In the